CLAIMS

We claim:

1. A phase detector generating either a first control signal or a second control signal responsive to a difference in phase between a first input signal and a second input signal, the phase detector comprising:

a signal comparator comparing the phase of the first input signal to the phase of the second input signal; and

a signal generator coupled to the signal comparator, the signal generator being operable to generate the first control signal responsive to the phase of the first input signal being greater than the phase of the second input signal by at least a first phase difference, and to generate the second control signal responsive to the phase of the first input signal being less than the phase of the second input signal by at least a second phase difference, the signal generator further being operable to generate neither the first control signal nor the second control signal responsive to either the first input signal being greater than the phase of the second input signal by less than the first phase difference or the first input signal being less than the phase of the second input signal by less than the second phase difference.

2. The phase detector of claim 1 wherein the first phase difference is substantially equal to the second phase difference.

3. The phase detector of claim 1 wherein the signal comparator comprises:

a first delay circuit having an output and an input coupled to receive the first input signal, the first delay circuit being operable to delay the first input signal by a first delay value and couple the delayed first input signal to the output;

a second delay circuit having an output and an input coupled to receive the second input signal, the second delay circuit being operable to delay the second input signal by a second delay value and couple the delayed second input signal to the output;

a third delay circuit having an output and an input coupled to receive the first input signal, the third delay circuit being operable to delay the first input signal by a third delay value and couple the delayed first input signal to the output;

a fourth delay circuit having an output and an input coupled to receive the second input signal, the fourth delay circuit being operable to delay the second input signal by a fourth delay value and couple the delayed second input signal to the output;

a first flip-flop having a set input coupled to the output of the first delay circuit, a reset input coupled to the output of the second delay circuit, and a pair of complimentary first and second outputs; and

a second flip-flop having a set input coupled to the output of the third delay circuit, a reset input coupled to the output of the fourth delay circuit, and a pair of complimentary first and second outputs.

4. The phase detector of claim 3 wherein the first delay value and the fourth delay value are substantially equal to each other.

5. The phase detector of claim 4 wherein the first delay value and the fourth delay value are substantially equal to a delay of zero.

6. The phase detector of claim 3 wherein the second delay value and the third delay value are substantially equal to each other.

7. The phase detector of claim 3 wherein the signal generator comprises:

a first output circuit having first and second inputs coupled to the first and second outputs of the first flip-flop, respectively, the first output circuit being operable to couple a first logic level to a first output when the first output of

the first flip-flop has the first logic level and the second output of the first flip-flop has a second logic level, to couple the first logic level to a second output when the second output of the first flip-flop has the first logic level and the first output of the first flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the flip-flop has the second logic level, and to couple the second logic level to the second output circuit when the second output of the first flip-flop has the second logic level;

a second output circuit having first and second inputs coupled to the first and second outputs of the second flip-flop, respectively, the second output circuit being operable to couple the first logic level to a first output when the first output of the second flip-flop has the first logic level and the second output of the second flip-flop has the second logic level, to couple the first logic level to a second output when the second output of the second flip-flop has the first logic level and the first output of the second flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the second flip-flop has the second logic level, and to couple the second logic level to the second output when the second output of the second flip-flop has the second logic level;

a first logic circuit having a first input coupled to the first output of the first output circuit, a second input coupled to the first output of the second output circuit, and an output on which the first control signal is generated; and

a second logic circuit having a second input coupled to the second output of the first output circuit, a second input coupled to the second output of the second output circuit, and an output on which the second control signal is generated.

8. The phase detector of claim 7 wherein the first logic circuit is operable to generate the first control signal responsive to both the first output of the first output circuit and the first output of the second output circuit having the first logic level, and wherein the second logic circuit is operable to generate the second control signal responsive to both the second output of the first output circuit and the second output of the second output circuit having the first logic level.

9. The phase detector of claim 8 wherein the first and second logic circuits each receive the first and second input signals, and wherein the first and second control signal are generated only if the first and second input signals have the first logic level.

10. A delay-lock loop, comprising:

a phase detector comparing the phase of a reference clock signal to the phase of a feedback clock signal, the phase detector being operable to generate an increase control signal responsive to the feedback clock signal leading the reference clock signal by at least a first delay time, and to generate a decrease control signal responsive to the feedback clock signal lagging the reference clock signal by at least a second delay time, the phase detector further being operable to generate neither the increase control signal nor the decrease control signal responsive to either the feedback clock signal leading the reference clock signal by less than the first delay time or the feedback clock signal lagging the reference clock signal by less than the second delay time;

a delay control circuit coupled to the phase detector, the delay control circuit generating a delay control signal responsive to the increase and decrease control signals from the phase detector; and

a delay circuit coupled to the delay control circuit, the delay circuit being coupled to receive the reference clock signal and to delay the reference clock signal by a variable delay to generate the feedback clock signal from the delayed reference clock signal, the delay circuit being operable to increase the magnitude of the variable delay responsive to a delay control signal generated

responsive to the increase control signal and to decrease the magnitude of the variable delay responsive to a delay control signal generated responsive to the decrease control signal.

11. The delay-lock loop of claim 10 wherein the first delay time is substantially equal to the second delay time.

12. The delay-lock loop of claim 10 wherein the phase detector comprises:

a first delay circuit having an output and an input coupled to receive the reference clock signal, the first delay circuit being operable to delay the reference clock signal by a first delay value and couple the delayed reference clock signal to the output;

a second delay circuit having an output and an input coupled to receive the feedback clock signal, the second delay circuit being operable to delay the feedback clock signal by a second delay value and couple the delayed feedback clock signal to the output;

a third delay circuit having an output and an input coupled to receive the reference clock signal, the third delay circuit being operable to delay the reference clock signal by a third delay value and couple the delayed reference clock signal to the output;

a fourth delay circuit having an output and an input coupled to receive the feedback clock signal, the fourth delay circuit being operable to delay the feedback clock signal by a fourth delay value and couple the delayed feedback clock signal to the output;

a first flip-flop having a set input coupled to the output of the first delay circuit, a reset input coupled to the output of the second delay circuit, and a pair of complimentary first and second outputs; and

a second flip-flop having a set input coupled to the output of the third delay circuit, a reset input coupled to the output of the fourth delay circuit, and a pair of complimentary first and second outputs.

13. The delay-lock loop of claim 12 wherein the first delay value and the fourth delay value are substantially equal to each other.

14. The delay-lock loop of claim 13 wherein the first delay value and the fourth delay value are substantially equal to a delay of zero.

15. The delay-lock loop of claim 12 wherein the second delay value and the third delay value are substantially equal to each other.

16. The delay-lock loop of claim 12 wherein the phase detector further comprises:

a first output circuit having first and second inputs coupled to the first and second outputs of the first flip-flop, respectively, the first output circuit being operable to couple a first logic level to a first output when the first output of the first flip-flop has the first logic level and the second output of the first flip-flop has a second logic level, to couple the first logic level to a second output when the second output of the first flip-flop has the first logic level and the first output of the first flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the flip-flop has the second logic level, and to couple the second logic level to the second output circuit when the second output of the first flip-flop has the second logic level;

a second output circuit having first and second inputs coupled to the first and second outputs of the second flip-flop, respectively, the second output circuit being operable to couple the first logic level to a first output when the first output of the second flip-flop has the first logic level and the second output of the second flip-flop has the second logic level, to couple the first logic level to a second output when the second output of the second flip-flop has the first logic level and the first output of the second flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the second flip-flop has the second logic level, and to couple the second logic level to the second output when the second output of the second flip-flop has the second logic level;

a first logic circuit having a first input coupled to the first output of the first output circuit, a second input coupled to the first output of the second output circuit, and an output on which the increase control signal is generated; and

a second logic circuit having a second input coupled to the second output of the first output circuit, a second input coupled to the second output of the second output circuit, and an output on which the decrease control signal is generated.

17. The delay-lock loop of claim 16 wherein the first logic circuit is operable to generate the increase control signal responsive to both the first output of the first output circuit and the first output of the second output circuit having the first logic level, and wherein the second logic circuit is operable to generate the decrease control signal responsive to both the second output of the first output circuit and the second output of the second output circuit having the first logic level.

18. The delay-lock loop of claim 17 wherein the first and second logic circuits each receive the reference clock signal and the feedback clock signal, and wherein the increase and decrease control signal are generated only if the reference clock signal and the feedback clock signal have the first logic level.

19. The delay-lock loop of claim 10 wherein the delay circuit is operable to increase the magnitude of the variable delay by a first delay increment responsive to the delay control signal generated responsive to the increase control signal and to decrease the magnitude of the variable delay by a second delay increment responsive to a delay control signal generated responsive to the decrease control signal.

20. The delay-lock loop of claim 19 wherein the first and second delay increments are each less than the sum of the first and second delay times.

21. A phase-lock loop, comprising:

a phase detector comparing the phase of a reference clock signal to the phase of a feedback clock signal, the phase detector being operable to generate an increase control signal responsive to the feedback clock signal leading the reference clock signal by at least a first time, and to generate a decrease control signal responsive to the feedback clock signal lagging the reference clock signal by at least a second time, the phase detector further being operable to generate neither the increase control signal nor the decrease control signal responsive to either the feedback clock signal leading the reference clock signal by less than the first time or the feedback clock signal lagging the reference clock signal by less than the second time;

a frequency control circuit coupled to the phase detector, the frequency control circuit generating a frequency control signal responsive to the increase and decrease control signals from the phase detector; and

a voltage controlled oscillator coupled to the frequency control circuit, the voltage controlled oscillator being operable to generate the feedback clock signal with a period that increases responsive to a frequency control signal generated responsive to the increase control signal and that decreases responsive to a frequency control signal generated responsive to the decrease control signal.

22. The phase-lock loop of claim 21 wherein the first time is substantially equal to the second time.

23. The phase-lock loop of claim 21 wherein the phase detector comprises:

a first delay circuit having an output and an input coupled to receive the reference clock signal, the first delay circuit being operable to delay the reference clock signal by a first delay value and couple the delayed reference clock signal to the output;

a second delay circuit having an output and an input coupled to receive the feedback clock signal, the second delay circuit being operable to delay

the feedback clock signal by a second delay value and couple the delayed feedback clock signal to the output;

a third delay circuit having an output and an input coupled to receive the reference clock signal, the third delay circuit being operable to delay the reference clock signal by a third delay value and couple the delayed reference clock signal to the output;

a fourth delay circuit having an output and an input coupled to receive the feedback clock signal, the fourth delay circuit being operable to delay the feedback clock signal by a fourth delay value and couple the delayed feedback clock signal to the output;

a first flip-flop having a set input coupled to the output of the first delay circuit, a reset input coupled to the output of the second delay circuit, and a pair of complimentary first and second outputs; and

a second flip-flop having a set input coupled to the output of the third delay circuit, a reset input coupled to the output of the fourth delay circuit, and a pair of complimentary first and second outputs.

24. The phase-lock loop of claim 23 wherein the first delay value and the fourth delay value are substantially equal to each other.

25. The phase-lock loop of claim 25 wherein the first delay value and the fourth delay value are substantially equal to a delay of zero.

26. The phase-lock loop of claim 24 wherein the second delay value and the third delay value are substantially equal to each other.

27. The phase-lock loop of claim 24 wherein the phase detector further comprises:

a first output circuit having first and second inputs coupled to the first and second outputs of the first flip-flop, respectively, the first output circuit being operable to couple a first logic level to a first output when the first output of the first flip-flop has the first logic level and the second output of the first flip-flop has a second logic level, to couple the first logic level to a second output

when the second output of the first flip-flop has the first logic level and the first output of the first flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the flip-flop has the second logic level, and to couple the second logic level to the second output circuit when the second output of the first flip-flop has the second logic level;

a second output circuit having first and second inputs coupled to the first and second outputs of the second flip-flop, respectively, the second output circuit being operable to couple the first logic level to a first output when the first output of the second flip-flop has the first logic level and the second output of the second flip-flop has the second logic level, to couple the first logic level to a second output when the second output of the second flip-flop has the first logic level and the first output of the second flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the second flip-flop has the second logic level, and to couple the second logic level to the second output when the second output of the second flip-flop has the second logic level;

a first logic circuit having a first input coupled to the first output of the first output circuit, a second input coupled to the first output of the second output circuit, and an output on which the increase control signal is generated; and

a second logic circuit having a second input coupled to the second output of the first output circuit, a second input coupled to the second output of the second output circuit, and an output on which the decrease control signal is generated.

28. The phase-lock loop of claim 27 wherein the first logic circuit is operable to generate the increase control signal responsive to both the first output of the first output circuit and the first output of the second output circuit having the first logic level, and wherein the second logic circuit is operable to generate the decrease control signal responsive to both the second output of the first output circuit and the second output of the second output circuit having the first logic level.

29. The phase-lock loop of claim 28 wherein the first and second logic circuits each receive the reference clock signal and the feedback clock signal, and wherein the increase and decrease control signal are generated only if the reference clock signal and the feedback clock signal have the first logic level.

30. The phase-lock loop of claim 21 wherein the voltage controlled oscillator is operable to increase the period of the feedback clock signal by a first time increment responsive to a frequency control signal generated responsive to the increase control signal, and that decreases by a second time increment responsive to a frequency control signal generated responsive to the decrease control signal.

31. The phase-lock loop of claim 30 wherein each of the first and second time increments is less than the sum of the first and second times.

32. A memory device, comprising:

a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;

a column address circuit operable to receive and decode column address signals applied to the external address terminals;

a memory cell array operable to store data written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;

a clock generator circuit operable to generate an output clock signal from a reference clock signal, the clock generator circuit comprising:

a phase detector comparing the phase of the reference clock signal to the phase of a feedback clock signal, the phase detector being operable to generate an increase control signal responsive to the feedback clock signal leading the reference clock signal by at least a first time, and to generate a decrease control signal responsive to the feedback clock signal lagging the reference clock signal by at least a second time, the

phase detector further being operable to generate neither the increase control signal nor the decrease control signal responsive to either the feedback clock signal leading the reference clock signal by less than the first time or the feedback clock signal lagging the reference clock signal by less than the second time;

a delay control circuit coupled to the phase detector, the delay control circuit generating a delay control signal responsive to the increase and decrease control signals from the phase detector; and

a delay circuit coupled to the delay control circuit, the delay circuit being coupled to receive the reference clock signal and to delay the reference clock signal by a variable delay to generate the output clock signal and the feedback clock signal from the delayed reference clock signal, the delay circuit being operable to increase the magnitude of the variable delay responsive to a delay control signal generated responsive to the increase control signal and to decrease the magnitude of the variable delay responsive to a delay control signal generated responsive to the decrease control signal;

a data path circuit operable to couple data signals corresponding to the data between the array and data bus terminals of the memory device, the data path circuit comprising a plurality of read data latches each having an input terminal coupled to the array, an output terminal coupled to a respective data bus terminal, and a clock terminal coupled to receive the output clock signal from the clock generator circuit, the read data latches being operable to couple read data bits from the output latch to the data bus terminals responsive to a transition of the output clock signal; and

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals.

33. The memory device of claim 32 wherein the first time is substantially equal to the second time.

34. The memory device of claim 32 wherein the phase detector comprises:

a first delay circuit having an output and an input coupled to receive the reference clock signal, the first delay circuit being operable to delay the reference clock signal by a first delay value and couple the delayed reference clock signal to the output;

a second delay circuit having an output and an input coupled to receive the feedback clock signal, the second delay circuit being operable to delay the feedback clock signal by a second delay value and couple the delayed feedback clock signal to the output;

a third delay circuit having an output and an input coupled to receive the reference clock signal, the third delay circuit being operable to delay the reference clock signal by a third delay value and couple the delayed reference clock signal to the output;

a fourth delay circuit having an output and an input coupled to receive the feedback clock signal, the fourth delay circuit being operable to delay the feedback clock signal by a fourth delay value and couple the delayed feedback clock signal to the output;

a first flip-flop having a set input coupled to the output of the first delay circuit, a reset input coupled to the output of the second delay circuit, and a pair of complimentary first and second outputs; and

a second flip-flop having a set input coupled to the output of the third delay circuit, a reset input coupled to the output of the fourth delay circuit, and a pair of complimentary first and second outputs.

35. The memory device of claim 34 wherein the first delay value and the fourth delay value are substantially equal to each other.

36. The memory device of claim 35 wherein the first delay value and the fourth delay value are substantially equal to a delay of zero.

37. The memory device of claim 35 wherein the second delay value and the third delay value are substantially equal to each other.

38. The memory device of claim 35 wherein the phase detector further comprises:

a first output circuit having first and second inputs coupled to the first and second outputs of the first flip-flop, respectively, the first output circuit being operable to couple a first logic level to a first output when the first output of the first flip-flop has the first logic level and the second output of the first flip-flop has a second logic level, to couple the first logic level to a second output when the second output of the first flip-flop has the first logic level and the first output of the first flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the flip-flop has the second logic level, and to couple the second logic level to the second output circuit when the second output of the first flip-flop has the second logic level;

a second output circuit having first and second inputs coupled to the first and second outputs of the second flip-flop, respectively, the second output circuit being operable to couple the first logic level to a first output when the first output of the second flip-flop has the first logic level and the second output of the second flip-flop has the second logic level, to couple the first logic level to a second output when the second output of the second flip-flop has the first logic level and the first output of the second flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the second flip-flop has the second logic level, and to couple the second logic level to the second output when the second output of the second flip-flop has the second logic level;

a first logic circuit having a first input coupled to the first output of the first output circuit, a second input coupled to the first output of the second output circuit, and an output on which the increase control signal is generated; and

a second logic circuit having a second input coupled to the second output of the first output circuit, a second input coupled to the second output of

the second output circuit, and an output on which the decrease control signal is generated.

39. The memory device of claim 38 wherein the first logic circuit is operable to generate the increase control signal responsive to both the first output of the first output circuit and the first output of the second output circuit having the first logic level, and wherein the second logic circuit is operable to generate the decrease control signal responsive to both the second output of the first output circuit and the second output of the second output circuit having the first logic level.

40. The memory device of claim 39 wherein the first and second logic circuits each receive the reference clock signal and the feedback clock signal, and wherein the increase and decrease control signal are generated only if the reference clock signal and the feedback clock signal have the first logic level.

41. The memory device of claim 32 wherein the delay circuit is operable to increase the magnitude of the variable delay by a first delay increment responsive to the delay control signal generated responsive to the increase control signal and to decrease the magnitude of the variable delay by a second delay increment responsive to a delay control signal generated responsive to the decrease control signal.

42. The memory device of claim 41 wherein each of the first and second delay increments is less than the sum of the first and second delay times.

43. The memory device of claim 34 wherein the memory cell array comprises a dynamic random access memory cell array.

44. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus to allow data to be output from the computer system;

a data storage device coupled to the processor through the processor bus to allow data to be read from a mass storage device; and

a memory device coupled to the processor, the memory device comprising:

a row address circuit operable to receive and decode row address signals applied to external address terminals of the memory device;

a column address circuit operable to receive and decode column address signals applied to the external address terminals;

a memory cell array operable to store data written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;

a clock generator circuit operable to generate an output clock signal from a reference clock signal, the clock generator circuit comprising:

a phase detector comparing the phase of the reference clock signal to the phase of a feedback clock signal, the phase detector being operable to generate an increase control signal responsive to the feedback clock signal leading the reference clock signal by at least a first time, and to generate a decrease control signal responsive to the feedback clock signal lagging the reference clock signal by at least a second time, the phase detector further being operable to generate neither the increase control signal nor the decrease control signal responsive to either the feedback clock signal leading the reference clock signal by less than the first time or the feedback clock signal lagging the reference clock signal by less than the second time;

a delay control circuit coupled to the phase detector, the delay control circuit generating a delay control signal responsive to the increase and decrease control signals from the phase detector; and

a delay circuit coupled to the delay control circuit, the delay circuit being coupled to receive the reference clock signal and to delay the reference clock signal by a variable delay to generate the output clock signal and the feedback clock signal from the delayed reference clock signal, the delay circuit being operable to increase the magnitude of the variable delay responsive to a delay control signal generated responsive to the increase control signal and to decrease the magnitude of the variable delay responsive to a delay control signal generated responsive to the decrease control signal;

a data path circuit operable to couple data signals corresponding to the data between the array and data bus terminals of the memory device, the data path circuit comprising a plurality of read data latches each having an input terminal coupled to the array, an output terminal coupled to a respective data bus terminal, and a clock terminal coupled to receive the output clock signal from the clock generator circuit, the read data latches being operable to couple read data bits from the output latch to the data bus terminals responsive to a transition of the output clock signal; and

a command decoder operable to decode a plurality of command signals applied to respective external command terminals of the memory device, the command decoder being operable to generate control signals corresponding to the decoded command signals.

45. The computer system of claim 44 wherein the first time is substantially equal to the second time.

46. The computer system of claim 44 wherein the phase detector comprises:

a first delay circuit having an output and an input coupled to receive the reference clock signal, the first delay circuit being operable to delay the reference clock signal by a first delay value and couple the delayed reference clock signal to the output;

a second delay circuit having an output and an input coupled to receive the feedback clock signal, the second delay circuit being operable to delay the feedback clock signal by a second delay value and couple the delayed feedback clock signal to the output;

a third delay circuit having an output and an input coupled to receive the reference clock signal, the third delay circuit being operable to delay the reference clock signal by a third delay value and couple the delayed reference clock signal to the output;

a fourth delay circuit having an output and an input coupled to receive the feedback clock signal, the fourth delay circuit being operable to delay the feedback clock signal by a fourth delay value and couple the delayed feedback clock signal to the output;

a first flip-flop having a set input coupled to the output of the first delay circuit, a reset input coupled to the output of the second delay circuit, and a pair of complimentary first and second outputs; and

a second flip-flop having a set input coupled to the output of the third delay circuit, a reset input coupled to the output of the fourth delay circuit, and a pair of complimentary first and second outputs.

47. The computer system of claim 46 wherein the first delay value and the fourth delay value are substantially equal to each other.

48. The computer system of claim 47 wherein the first delay value and the fourth delay value are substantially equal to a delay of zero.

49. The computer system of claim 46 wherein the second delay value and the third delay value are substantially equal to each other.

50. The computer system of claim 46 wherein the phase detector further comprises:

a first output circuit having first and second inputs coupled to the first and second outputs of the first flip-flop, respectively, the first output circuit being operable to couple a first logic level to a first output when the first output of the first flip-flop has the first logic level and the second output of the first flip-flop has a second logic level, to couple the first logic level to a second output when the second output of the first flip-flop has the first logic level and the first output of the first flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the flip-flop has the second logic level, and to couple the second logic level to the second output circuit when the second output of the first flip-flop has the second logic level;

a second output circuit having first and second inputs coupled to the first and second outputs of the second flip-flop, respectively, the second output circuit being operable to couple the first logic level to a first output when the first output of the second flip-flop has the first logic level and the second output of the second flip-flop has the second logic level, to couple the first logic level to a second output when the second output of the second flip-flop has the first logic level and the first output of the second flip-flop has the second logic level, to couple the second logic level to the first output when the first output of the second flip-flop has the second logic level, and to couple the second logic level to the second output when the second output of the second flip-flop has the second logic level;

a first logic circuit having a first input coupled to the first output of the first output circuit, a second input coupled to the first output of the second output circuit, and an output on which the increase control signal is generated; and

a second logic circuit having a second input coupled to the second output of the first output circuit, a second input coupled to the second output of

the second output circuit, and an output on which the decrease control signal is generated.

51. The computer system of claim 50 wherein the first logic circuit is operable to generate the increase control signal responsive to both the first output of the first output circuit and the first output of the second output circuit having the first logic level, and wherein the second logic circuit is operable to generate the decrease control signal responsive to both the second output of the first output circuit and the second output of the second output circuit having the first logic level.

52. The computer system of claim 41 wherein the first and second logic circuits each receive the reference clock signal and the feedback clock signal, and wherein the increase and decrease control signal are generated only if the reference clock signal and the feedback clock signal have the first logic level.

53. The computer system of claim 44 wherein the delay circuit is operable to increase the magnitude of the variable delay by a first delay increment responsive to the delay control signal generated responsive to the increase control signal and to decrease the magnitude of the variable delay by a second delay increment responsive to a delay control signal generated responsive to the decrease control signal.

54. The computer system of claim 53 wherein each of the first and second delay increments is less than the sum of the first and second delay times.

55. The computer system of claim 44 wherein the memory cell array comprises a dynamic random access memory cell array.

56. A method of controlling the operation of a delay-lock loop in which a reference clock signal is delayed by a delay value to generate a feedback clock signal, the method comprising:

comparing the phase of the reference clock signal to the phase of the feedback clock signal;

increasing the delay value responsive to the feedback clock signal leading the reference clock signal by at least a first time duration;

decreasing the delay value responsive to the feedback clock signal lagging the reference clock signal by at least a second time duration; and

maintaining the delay value substantially the same responsive to either the feedback clock signal leading the reference clock signal by less than the first time duration or the feedback clock signal lagging the reference clock signal by less than the second time duration.

57. The method of claim 56 wherein the first time duration is substantially equal to the second time duration.

58. The method of claim 56 wherein the act of increasing the delay value responsive to the feedback clock signal leading the reference clock signal by at least a first time duration comprises increasing the delay value by a first delay increment, and wherein the act of decreasing the delay value responsive to the feedback clock signal lagging the reference clock signal by at least a second time duration comprises decreasing the delay value by a second delay increment.

59. The method of claim 58 wherein each of the first and second delay increments is less than the sum of the first and second time durations.